

CLAIMS

What is claimed is:

- 1 1. An apparatus comprising:
 - 2 a first wafer having a first interlayer dielectric layer and a first plurality of
 - 3 copper structures of first substantially uniform heights with each difference
 - 4 between any two of the first substantially uniform heights being 5 nm or less,
 - 5 disposed on the first interlayer dielectric layer; and
 - 6 a second wafer having a second interlayer dielectric layer and a second
 - 7 plurality of copper structures of second substantially uniform heights with each
 - 8 difference between any two of the second substantially uniform heights being
 - 9 5nm or less, disposed on the second interlayer dielectric layer,, the second wafer
 - 10 being stacked on the first wafer, with at least some of the first and second
 - 11 plurality of cooper structures being substantially aligned and bonded to each
 - 12 other.
 - 13
- 1 2. The apparatus of claim 1, wherein at least a selected one of the first and
- 2 second substantially uniform heights is in a range of 100-300nm.
- 3
- 1 3. The apparatus of claim 2, wherein both the first and second substantially
- 2 uniform heights are in the range of 100-300nm.
- 3
- 1 4. A method comprising:
 - 2 providing a first wafer comprising first copper structures encased in a first
 - 3 interlayer dielectric layer; and

4 wet etching the first wafer to expose the first copper structures with the
5 first copper structures having first substantially uniform heights, where each
6 difference between any two of the first substantially uniform heights is 5 nm or
7 less.

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1 5. The method of claim 4, wherein the etching comprises etching the first
2 wafer using a diluted organic hydrofluoric acid, assisted by a super critical CO₂ to
3 remove part of the interlayer dielectric layer.

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1 6. The method of claim 5, further comprises rinsing the first wafer with
2 deionized water.

1 7. The method of claim 4, wherein the etching comprises etching the first
2 wafer using a diluted hydrofluoric acid to selectively remove part of the interlayer
3 dielectric layer.

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1 8. The method of claim 4, wherein the etching comprises etching the first
2 wafer using an ethylene glycol based solution and a diluted hydrofluoric acid to
3 remove part of the interlayer dielectric layer.

1 9. The method of claim 4, wherein the etching comprises etching the first
2 wafer using a buffered oxide etch reactant to remove parts of the interlayer
3 dielectric layer.

1 10. The method of claim 4, wherein the etching comprises etching the wafer
2 using a buffered oxide etch reactant and a diluted hydrofluoric acid to remove
3 part of the interlayer dielectric layer.

1 11. The method of claim 4, wherein the etching comprises etching the wafer
2 using a buffered oxide etch reactant, an ethylene glycol based solution and a
3 diluted hydrofluoric acid to remove part of the interlayer dielectric layer.

1 12. The method of claim 4, wherein the method further comprises performing
2 a reactive pre-cleans using hydrogen-based plasma to remove residues on a
3 surface of the copper structures. .

1 13. The method of claim 4, wherein the method further comprises
2 providing a second wafer comprising second copper structures encased in
3 a second interlayer dielectric layer; and
4 wet etching the second wafer to expose the second copper structures with
5 the second copper structures having second substantially uniform heights, where
6 each difference between any two of the second substantially uniform heights is 5
7 nm or less.

1 14. The method of claim 13, wherein the method further comprises
2 aligning the first and second wafers; and
3 bonding at least some of the first copper structures to some of the second
4 copper structures to bond and stack the first wafer on the second wafer.

1 15. A system comprising:

2 a semiconductor package having
3 a first die having a first interlayer dielectric layer and a first plurality of
4 copper structures of first substantially uniform heights disposed on
5 the first interlayer dielectric layer, where each difference between
6 any two of the first substantially uniform heights is 5 nm or less; and
7 a second die having a second interlayer dielectric layer and a second
8 plurality of cooper structures of second substantially uniform
9 heights disposed on the second interlayer dielectric layer, where
10 each difference between any two of the two substantially uniform
11 heights is 5 nm or less, the second die being stacked on the first
12 die, with at least some of the first and second plurality of cooper
13 structures being substantially aligned and bonded to each other;
14 a bus coupled to the semiconductor package; and
15 a networking interface component coupled to the bus.

1 16. The system of claim 15, wherein at least a selected one of the first and
2 second substantially uniform heights of the semiconductor package is in a range
3 of 100-300nm.

1 17 The system of claim 16, wherein both of the first and second substantially
2 uniform heights of the semiconductor package is in the range of 100-300nm.

1 18. The system of claim 15, wherein the system is a selected one of a digital
2 versatile disk player and a set-top box.